THAT WHICH IS CLAIMED IS:

1. Semiconductor device with MOS transistors, comprising a semiconductor substrate (10) in which the transistors are formed, a dielectric layer (14) which covers the substrate and in which contact holes (16) are etched, and an etch-stop layer (18) interposed between the substrate and the dielectric layer, characterized in that the etch-stop layer includes a first layer (I) of material which has a first residual stress level and covers some of the transistors, and a second layer (II) of material which has a second residual stress level and covers all of the transistors, the thicknesses (e1, e2) of the first and second layers, and the first and second residual stress levels (σ_1, σ_2), being selected so as to obtain variations in operating parameters of the transistors with respect to transistors covered by the first layer of material.

2. Device according to Claim 1, characterized in that the MOS transistors include NMOS-type transistors and PMOS-type transistors, and in that the first and second layers of material (I, II) have opposite residual stress levels.

3. Device according to Claim 2, characterized in that the thicknesses (e1, e2) of the first layer and of the second layer, and the residual stress levels (σ_1, σ_2) of the first layer and of the second layer, are determined so as to obtain a positive stress level above the NMOS transistors and a negative stress level above the PMOS transistors.

4. Device according to one of Claims 2 and 3, characterized in that the first layer has a negative stress level and covers the PMOS-type transistors, and the second layer has a positive stress level.

5. Device according to one of Claims 2 and 3, characterized in that the first layer has a positive stress level and covers the NMOS-type transistors, and the second layer has a negative stress level.

6. Device according to any one of Claims 1 to 5, characterized in that the zone of the second layer covering the first layer has a substantially zero residual stress.

7. Method for fabricating a semiconductor device with MOS transistors according to any one of Claims 1 to 6, comprising formation of the transistors in a semiconductor substrate (10), deposition of an etch-stop layer (18) on the transistors, deposition of a dielectric layer on the etch-stop layer and etching of connection holes in the dielectric layer, characterized in that the step of depositing the etch-stop layer comprises the deposition of a first layer (I) of material which has a first residual stress level and covers some of the transistors, and the deposition on the first layer of a second layer (II) of material which has a second residual stress level and covers all of the transistors, the thicknesses of the first and second layers, and the first and second residual stress levels, being selected so as to obtain variations in operating parameters of the transistors with respect to

transistors covered by the first layer of material.

8. Method according to Claim 7, characterized in that the step of depositing the first layer involves deposition of the said layer on all of the transistors, deposition of masks at the positions of the transistors of the said some of the transistors, etching of the exposed layer and removal of the masks.

9. Method according to one of Claims 7 and 8, characterized in that, subsequent to the step of depositing the second layer, a localized treatment of the material of the second layer (II) is carried out at the positions of the transistors of the said some of the transistors so as to locally modify the stress level of the second layer.

10. Method according to Claim 9, characterized in that the treatment of the second layer is carried out by ion implantation.

11. Method according to Claim 10, characterized in that the treatment of the second layer is carried out by ion implantation of Ge.